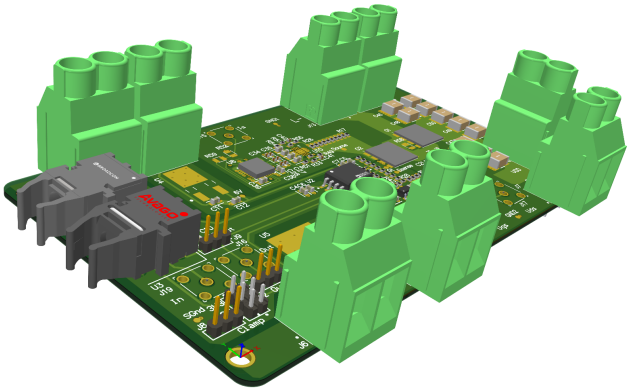
Characterizing the Performance of GaN FETs



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EXECUTIVE SUMMARY

As the performance of silicon based MOSFETs are approaching their limitations, a new type of transistor is necessary to pioneer the next generation of power electronics. Our sponsors are interested in Gallium Nitride FETs, a new type of transistor which has been shown in research to have a significantly higher performance potential than conventional MOSFETs. Our team's task is to characterize the performance of GaN FETs under high voltage and high speed situations, ultimately studying its efficacy in power electronics.

To do so, we use the industry standard Double Pulse Test (DPT) circuit to test the GaN FETs under various voltages. Moreover, we use a specific GaN FET gate driver to properly drive the FET within a suitable operating range in our DPT. To capture waveforms of the signals on the PCB, our design includes on board measurement circuits to provide high bandwidth measurements without affecting signal integrity. Our board allows us to analyze the waveforms on the DPT to retrieve performance parameters such as the switching time and power losses.

The current DPT PCB is manufactured but has not been used for testing yet. Once done, a characterization of the measurement circuitry should be conducted to validate the performance of our designs. Furthermore, for GaN FETs to be adopted into industry, thermal tests under high frequency repeated switching is required in order to verify its usability in real world operations.

INTRODUCTION

The sponsors for our project are Professor William Dunford, Dr. Ahmed Sherwali, and Professor Patrick Palmer. Professor Dunford is part of the Electrical and Computer Engineering Department at UBC and focuses in energy efficiency and smart grid area. Dr. Sherwali is a PhD graduate under Professor Dunford researching new oil extraction methods using electromagnetic induction. Professor Palmer is part of the School of Mechatronic Systems Engineering at SFU specializing in power semiconductor device research and driver design. Our sponsors are interested in understanding the performance of Gallium Nitride Field Effect Transistors (GaN FETs) for their research in high speed power electronics.

Sponsors Objective

Our sponsors' objective is to characterize the performance of GaN FETs, and to design a H-Bridge using these FETs to drive an inductive load. Our main objective is to design characterization circuitry that measures performance parameters of the FETs, and to evaluate how circuit design affects those parameters.

Background and Significance

Silicon based transistors are the current industry standard in power electronics. Significant improvement has been made to these transistors over the past decades; the package size, switching speeds, and internal resistances have improved dramatically. However, silicon semiconductors are reaching their physical limits. Hence, the next-generation of transistors must be made of new materials like gallium nitride (GaN). GaN field effect transistors (GaN FETs) are more efficient, can be operated significantly faster, and are much smaller compared to traditional MOSFETs. This revolutionary new technology is on the verge of dominating power electronics.

Although these novel FETs demonstrate high potential to revolutionize power electronics, accurate characterization of the switching loss and transients are necessary to be able to reliably use GaN FETs in new designs [19]. This characterization is a difficult problem to solve due to the nature of high speed high voltage electronics, and the errors from measurement circuitry.

Statement of Problem

The goal of our project is to characterize GaN FET switching parameters - the rise times, fall times, and power losses during a switch. This requires designing a Double Pulse Test circuit to switch the FETs at desired voltages and speeds as well as designing precise measurement circuitry able to capture high frequency ringing components critical to our performance calculations. We will also analyze how to tune the circuit, specifically the gate resistance, to identify the optimal balance between minimal power loss and fast switching.

Scope and Limitations

At its inception, this project was based on developing a ‘test platform’ to explore the performance of GaN FETs. Our primary objective was to create an H-bridge capable of switching 600V at 1MHz. This H-bridge would be capable of delivering at least 30A, and would employ these GaN FETs to test them under intense operating conditions.

However, as we worked on this project, it became clear that a larger focus was needed on the characterization of the GaN FETs than originally anticipated. Although our sponsors’ ultimate goal stayed consistent, it became apparent that more concrete knowledge of our GaN FETs would be needed to attach any meaning to our results. Thus, our role shifted from being application oriented, to a deep analysis of the switching characteristics of the FETs to understand their behavior for use in future applications.

Our final scope table is thus modified to reflect the large changes to our project.

	Must Have	**Should Have**	**Nice to Have**
GaN FET	● Package Requirements (Vds Breakdown > 600V, 30A) ● Clearly Characterized Rise Time ● Clearly Characterized Switching Losses	● Rise Time < 10 ns ● Minimize Switching Losses (< Si MOSFETs)	● High Temperature Tolerance
Double Pulse Test Circuit	● Printed and Populated ● Proven accuracy through use		
Measurement Circuits	● Printed and Populated ● Bandwidth > 200 MHz ● Proven accuracy through use		
H-Bridge		● Design & Simulations	● Printed and Populated

Table 1. Finalized Scope Table for Project.

DISCUSSION

Theory

FET Switching Basics

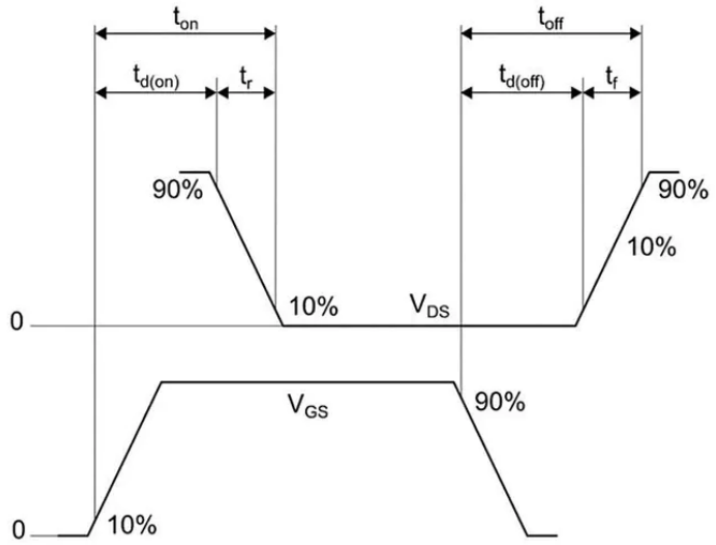

Figure 1. Turn on and turn off waveforms. Source: [Electronic Design](#).

Whenever a FET transitions from an on to an off state or vice-versa, there is a period during which there is both a voltage drop across, as well as current flowing through the FET. During this transition, power is dissipated as heat inside the FET. In addition to lowering the efficiency of the circuit, this energy lost as heat can damage or alter the performance of a FET [20].

In order to minimize energy loss during switching and reduce heating, we need to turn a FET on and off as fast as possible. Furthermore, in high-speed power electronics applications where timing is important, we also require fast switching. As such, switching speed is one of the key heuristics we use for characterizing the performance of FETs. The switching speed is limited by how quickly the parasitic (appendix A8) gate capacitance can be charged to a suitable voltage.

GaN FETs

Gallium nitride Field Effect Transistors or GaN FETs are high performance power transistors made out of gallium nitride. These transistors have superior characteristics when compared to conventional silicon power MOSFETs. An ideal power transistor would have:

- Low conduction losses
- Low switching losses
- High voltage ratings
- Strong thermal properties
- Small size

GaN FET performance is superior to that of silicon in all of these categories due to the intrinsic material properties of GaN and the specialized device FET architecture employed (see appendix A4). In electrical terms, this superiority can be understood as lower on resistance in the device, lower parasitic capacitances, and smaller devices for a given voltage rating. GaN FETs also generate less heat during operation due to the lower on resistance and parasitic capacitances causing lower power losses and so they have superior thermal properties compared to silicon. Further explanation of the physics behind GaN FETs can be found in the appendix A4.

Due to the physics of the GaN FETs, they can switch roughly 30 times faster than silicon power MOSFETs [11] (see appendix A4). This quality in particular is the focus of our studies for this project. The complexity of the analysis on GaN FETs and their driving circuits due to parasitic elements makes exact calculations of the switching speeds in a given application impossible. Therefore, we must determine switching parameters experimentally. We have been tasked by our sponsors to build a characterization platform to measure the switching performance of these GaN FETs in conditions which resemble conditions which our sponsors wish to study for their research.

Design and Methodology

Double Pulse Test

The industry standard circuit used to characterize switching performances of transistors is called the Double Pulse Test (DPT) [19]. Switching is done using an inductive load to simulate “hard switching” scenarios and a power supply to charge the inductor. A gate driver is used to turn the FET on and off.

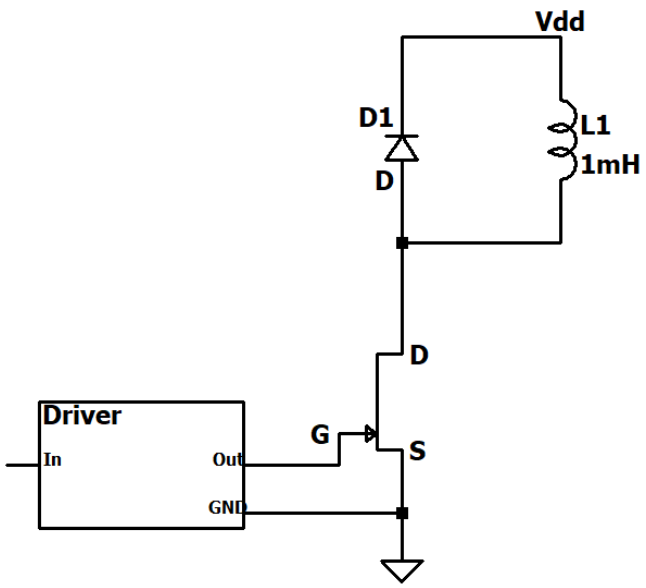

Figure 2. Example Double Pulse Test circuit schematic.

The double pulse test has 4 stages of operation. Initially the FET, which is the device under test (DUT), is in the off state and no current flows anywhere. In the first stage, the gate driver applies a high voltage to the gate of the DUT, turning it on, and current is allowed to begin building up in the path from V_{DD}, through the inductor, through the DUT to ground.

When the current has built up to a desired amount, stage two commences and the DUT is switched off. This simulates a “hard switch”, meaning the DUT goes from high to no current flowing through it in as little time as possible. Due to the miller effect [14], hard switching provides the most difficult conditions for switching. As such, it results in the longest possible turn off/on times, and worst case power dissipation in the FETs. The majority of FETs in power electronics are used while hard switching, and so it is imperative to understand device behaviour during these conditions.

During the second stage, after the DUT has been turned off, current continues to flow through the inductor, and up through a flyback diode. This stage lasts for long enough so that the DUT is in the off state. Since the time scale is so small, the current flowing through the inductor does not decay appreciably.

For stage three, the DUT is turned back on. The amount of current flowing through the inductor continues, but current now goes through the DUT instead of the flyback diode. This simulates a hard turn on. Once the DUT is on, the test is concluded, and the DUT is shut off.

In summary, the DPT provides the conditions to observe both a hard off and on switch. The overall voltage and current gate-source and drain-source waveforms of the FET can be seen in figure 3. These waveforms can be used to generate all the switching parameters we wish to study.

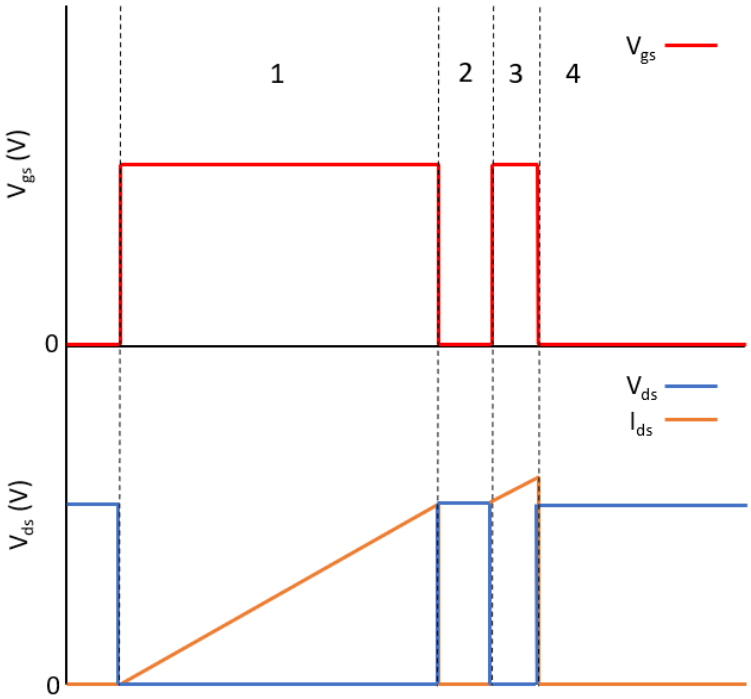

Figure 3. Double pulse test example waveforms.

It should be noted that in our DPT, we use an additional GaN FET on the highside in place of a flyback diode. This is possible due to the reverse conduction property which GaNs possess (see appendix A4). This allows us to observe and characterize reverse conduction as part of our testing.

Gate Driver Circuitry

The goal of the double pulse test is to characterize the performance of GaN Fets under the same fast conditions seen in a typical power electronics application. Thus, we must design effective driver circuitry to push the switching performance of the FET.

Our driver circuitry must turn the FET on and off. Bringing the gate to a suitably high voltage relative to the source (V_{GS}) turns the FET on and allows it to conduct. Due to the FETs parasitic capacitance (see appendix A8), a suitable amount of charge must be applied to achieve the desired V_{GS}. Our GaN FET requires 5.8 nC of charge to be applied to the gate in order to reach the desired V_{GS} of 6V [8]. In order to achieve a 10ns rise time on V_{GS}, an average current of 0.58A must be supplied.

There are several other important specifications for the driver circuitry. Large high speed transient voltages and currents can cause voltage and current to be induced at points throughout the circuit. If enough voltage couples to the gate, a false turn on may occur. Thus it is beneficial to have a low impedance path between the gate and the source when off [9]. With rapidly changing voltages and currents around the DUT, isolation between the control signal and driving circuitry is required [16].

The driver circuitry specifications are summarized as follows:

- 6V V_{GS} on
- Minimum rise time (ideally less than 10ns)
- Low R_{GS} off
- Provide Isolation between control and V_{GS}

Using these criteria and based on current availability from supplies, the ADuM4121 isolated driver was selected.

ADuM4121 Features [2]:

- 6V V_{GS} On
- 2A current sourcing/sinking
- 5kV rms Isolation between input and output.
- Miller clamp feature allows for low R_{GS} off.
- Ability to switch GaN FET at 1MHz

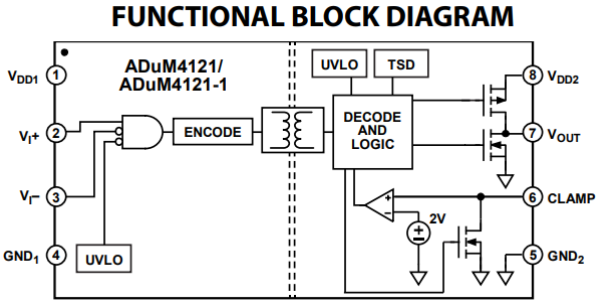

Figure 4. Functional block diagram. Source: [2].

Parasitic elements affect the gate drive loop of circuit by limiting the speed at which we are able send current to the FET, and by causing ringing. The primary source of capacitance is in the gate drive circuit is from the FET itself. Our GaN FETs have a gate-source capacitance of approximately 967pF [8]. The inductance which appears is proportional to the loop area of the gate drive loop [10]. The presence of this parasitic inductance increases the time it takes for current to start flowing in the loop meaning charge cannot be moved to or from the gate as easily, and switching speed is decreased [20]. Inductance is minimized by reducing the loop area by decreasing the distance between the driver and gate of the FET, and providing a close return path for current to flow from the driver to the FET.

Lastly, the existence of these parasitics results in the gate drive circuit forming a resonant RLC circuit. Attempting to quickly turn on the FET by inputting a step voltage excites the circuit near its natural frequency which causes oscillations in V_{GS}.

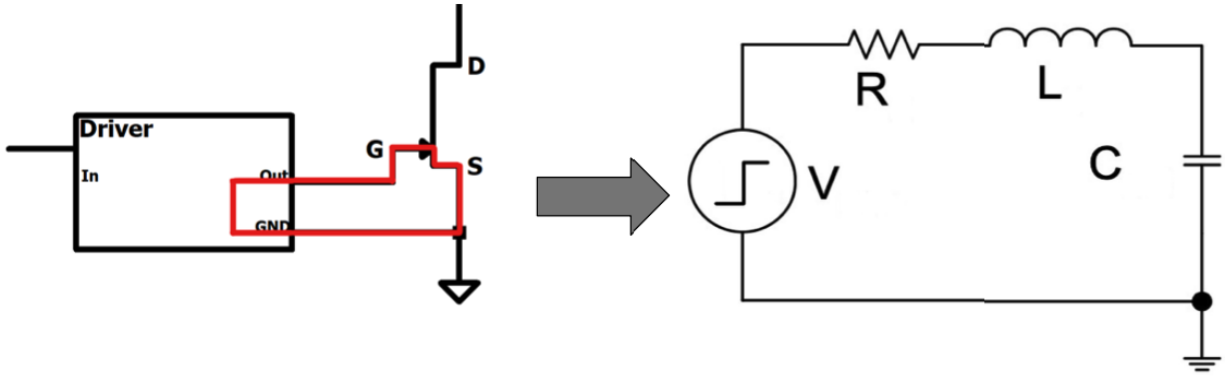

Figure 5. Gate drive loop shown to the left in red. Corresponding RLC equivalent circuit model shown right.

These oscillations have severe consequences. Firstly, the FETs we use have a maximum V_{GS} of 7.5V, and overshooting can permanently damage them. Next, if the oscillations cause the gate voltage to barely drop below the turn on threshold, the device will rapidly alternate between being on and off. Lastly, high frequency ringing on the gate causes unwanted high frequency EM radiation, which can couple into our other circuitry and cause unwanted behaviour. Our simulations have demonstrated that this ringing can be at frequencies up to 300 MHz, so we require proper measurement techniques in order to observe it.

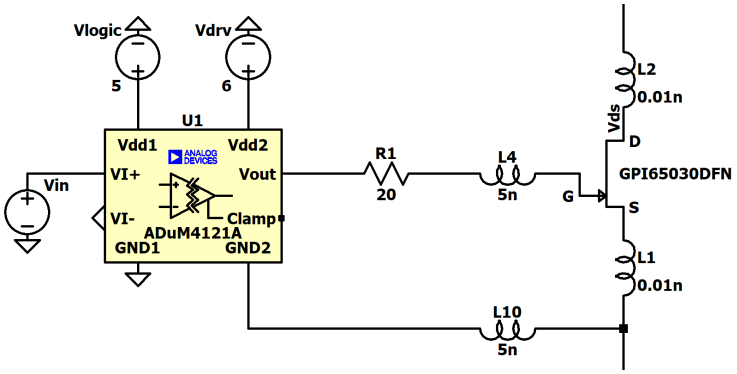

Figure 6. Basic gate drive topology LTspice model with parasitic inductance.

When designing the gate drive loop, our goal is to turn on our FET as fast as possible while avoiding excessive ringing. This balance can be tuned by adjusting the gate resistance. A lower gate resistance causes a faster turn on time. The tradeoff is higher overshoot and longer ringing [9]. Figure 6 shows the basic gate driver topology along with parasitic inductance of the gate drive loop. The DPT was simulated in LTspice with various gate resistances (R1 in figure 6). The results in figure 7 show how the gate resistance affects rise/fall time and overshoot. The parasitics which cause the overshoot and ringing of the circuit depend on the PCB layout and are difficult to estimate. For the simulations, estimates are taken from literature for typical gate drive loops [2]. The optimal gate resistance value should be determined experimentally.

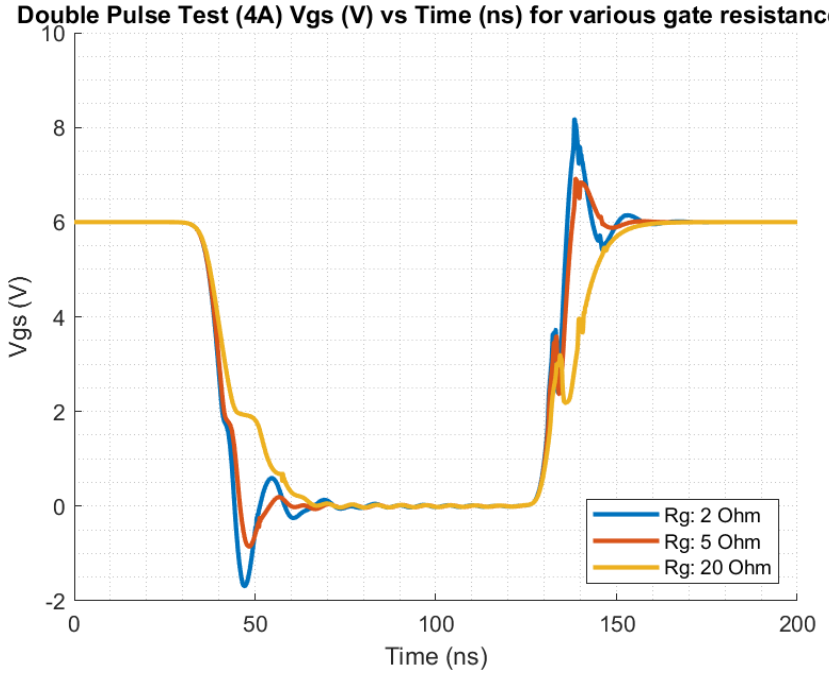

Figure 7. Showing the simulated V_{GS} switching waveforms from the double pulse test (DPT). The effect of the gate resistance on the rise/fall times and overshoot is clearly visible. It should also be noted that the blue waveform (R_G: 2Ω) exceeds the maximum V_{GS} and will damage the FET.

While the maximum positive V_{GS} of GaN FET we selected is 7.5V the maximum negative V_{GS} is -12V. This extra margin allows for larger overshoot on the falling waveform. A diode in series with another resistor is added in parallel with the normal gate resistor. The resulting circuit lowers the gate resistance while turning off, and decreases fall time [9]. Figure 9 shows the effect the diode has on the switching waveform.

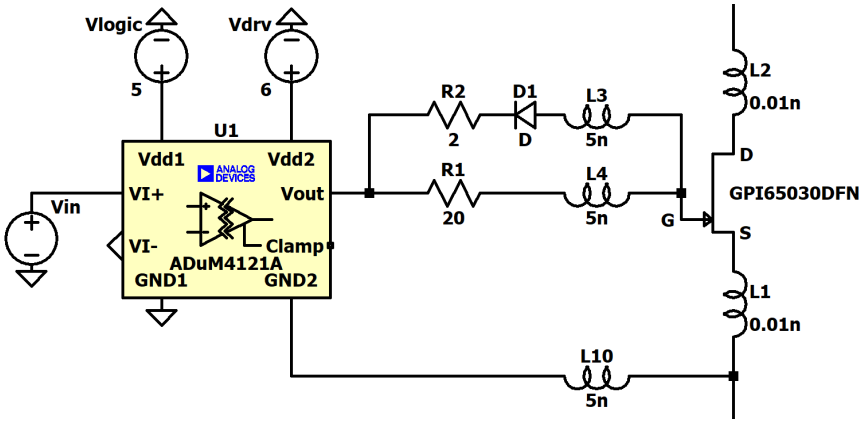

Figure 8. Modifications to the gate drive circuitry to lower the turn off resistance. The inductors represent parasitics.

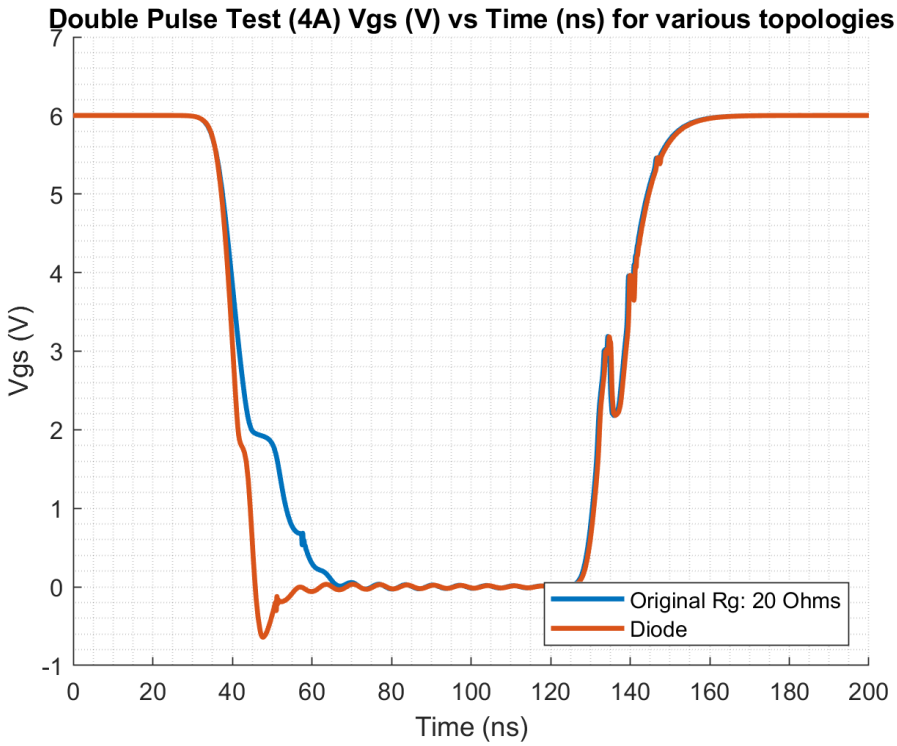

Figure 9. Depicting the effect of adding a diode to the gate drive loop. Due to the different gate on and off resistances, a faster turn off time is permitted. 2Ω resistance is used in series with the diode.

The overall driver circuitry is outlined in figure 10. 3 resistors are placed in parallel allowing for fine tuning of the main gate resistance. The 10 resistors in parallel just before the gate form a current shunt.

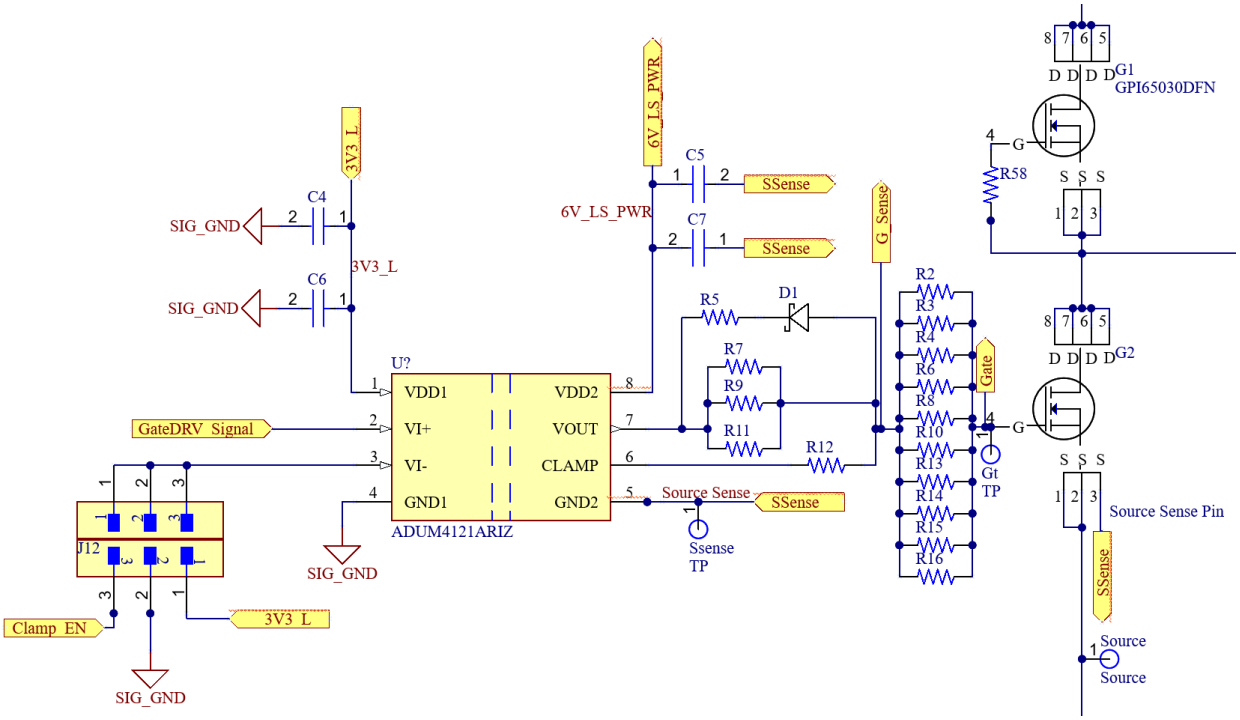

Figure 10. Full driver circuitry schematic as implemented on the PCB.

Measurement Circuitry

Conventionally, passive voltage probes are used to capture various signals on a PCB. The issue with parasitic elements arises again as a probe has inductance, capacitance and resistance, meaning the probe forms an RLC circuit with a resonant frequency. Attempting to measure a signal with frequency components at or higher than the probe's resonant frequency will result in an incoherent measurement, so all probes have a natural undistorted bandwidth limit. Our simulations suggest we could see ringing up to 300MHz and considering that active high bandwidth probes are expensive, we need an alternative solution.

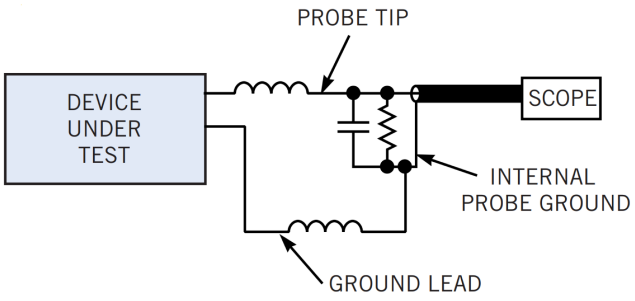

Figure 11. RLC circuit in a measurement probe. Source: [15MS512.QXD (edn.com)](15MS512.QXD (edn.com)).

Current Measurement Circuit

To characterize the board, we need to make two current measurements: I_{DS} and I_{GS}. Measuring currents is challenging because of added loop inductances.. Conceptually, current is measured indirectly by measuring the voltage drop across a shunt resistor. It is imperative to design a resistive shunt with low inductance and minimal resistive power loss. In practice, this means placing many small resistors in parallel [17].

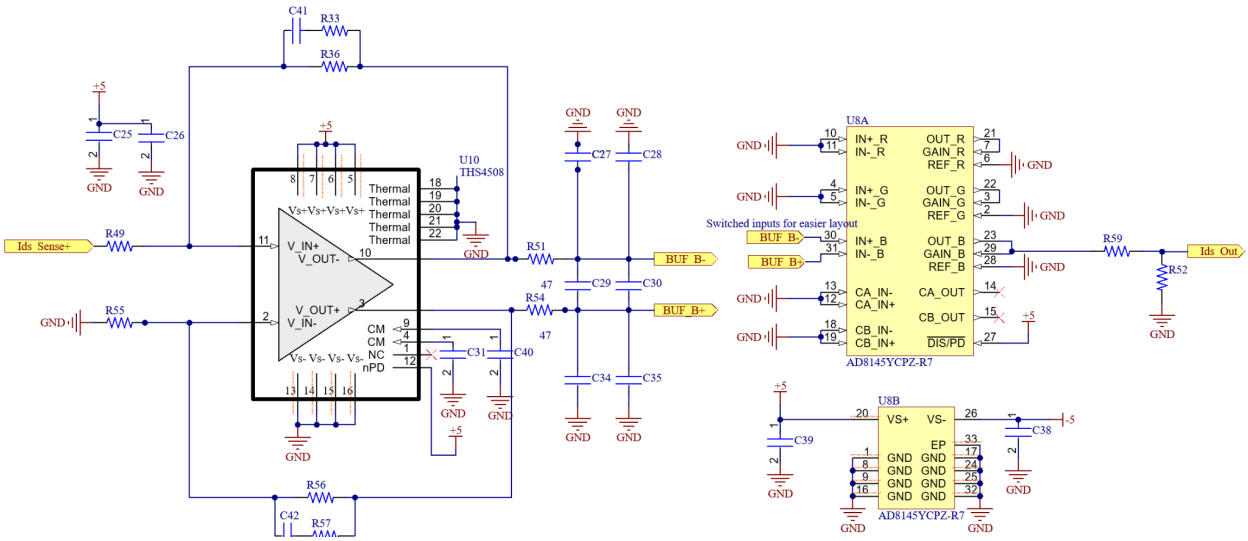

Figure 12. Current Measurement Schematic.

We use a two stage differential measurement circuit to provide high bandwidth differential measurements to mitigate excessive common mode noise. In the first stage, a THS4508 differential amplifier IC is used.

In the next stage, we use an AD8145 differential to single ended receiver. This component has an excellent common-mode rejection ratio, wide input common mode range, and high impedance inputs. Due to the high common-mode rejection ratio, any common mode noise in the signals is rejected.

This high performance circuit is optimal for all our current measurements, but is only used to measure I_{DS}. The reason is because the voltage levels at the gate of the DUT is outside of the operating range of the THS4508 component. Moreover, the loading due to the op-amp is significant and would affect the charge time of the gate. To measure I_{GS}, we decided to take

single ended voltage measurements across our gate shunt resistors. Since we are already measuring the voltage at the gate, we can use that as well to measure I_{GS}.

Voltage Measurement Circuit

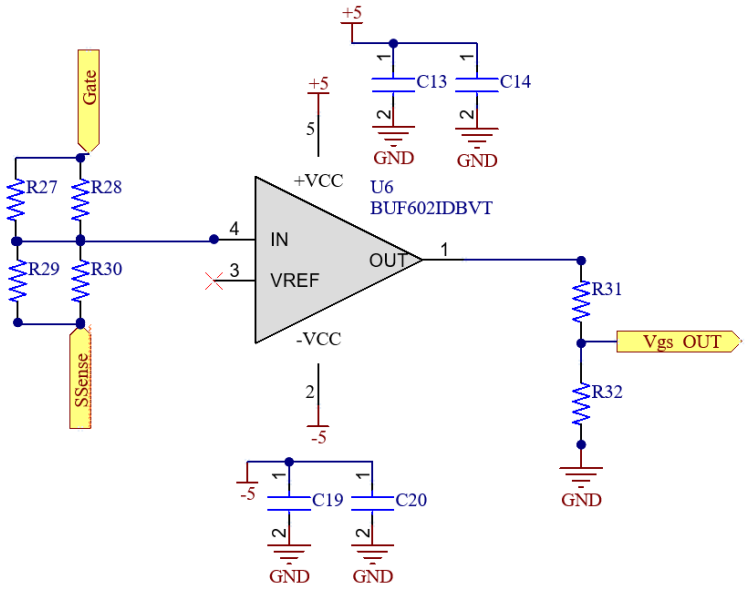

Figure 13. Voltage measurement circuit.

For our tests, we need to measure V_{DS} and V_{GS}. We require high bandwidth measurements in order to capture the ringing and voltage overshoot during switching. Some important design considerations are to minimize parasitic loading and power dissipation. The solution is to use a high impedance, high bandwidth closed loop buffer - we chose the BUF602.

In our DPT, we require all our buffers to have variable voltage dividers to lower the voltage to a suitable operating range. In practice, these resistors switch between tests since we conduct the DPT with various voltage supplies.

PCB Design

We designed our DPT circuit and measurement systems onto a PCB. Our PCB has 4 layers in this order: signal, ground, positive power, and negative power. The ground layer is right below the signal layer so that the return path of current is shorter, which minimizes the inductance of various loops in our circuit. Sensitive components such as the differential

amplifiers, gate driver, and GaN FETs have specific layout recommendations highlighted in their datasheets. Other important considerations in the layout process are highlighted below.

Via Placements

In high speed designs, improper via placements can introduce noise and corrupt signal or power integrity. It is best to avoid using vias to have signals switch layers since they add inductance to signal paths. However, placing sufficiently many vias to ground, like the ones used for the decoupling capacitors, creates a stronger connection, minimizes impedance, and shortens return loops [6].

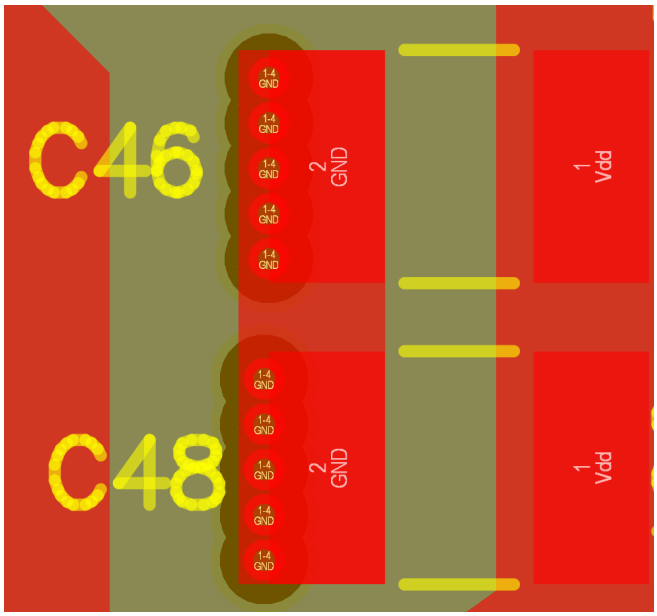

Figure 14. Optimal stitching via placement.

Differential Signals

Routing the PCB also requires various considerations. Beside ensuring power traces are wide enough, the lengths of differential signal pairs should be matched. An example is shown in figure 15. The traces leading into and out of the first stage differential amplifier (shown on the right half) ideally have the same lengths ensuring matched impedances and matched signal propagation times. Any impedance or propagation delay mismatches will cause common-mode voltages to be amplified, affecting the integrity of the resulting signal.

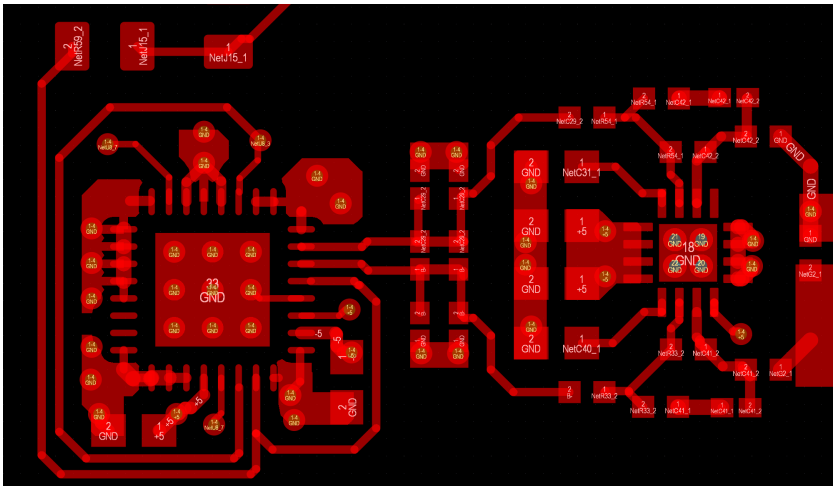

Figure 15. Symmetrical traces in the current measurement circuit.

Polygon Pours

We make use of many polygon pours in our PCB layout. These are used for the switching node (drain of the DUT), and the source of the DUT. This is shown in the figure below as the right and left red pours respectively. Notice that we cut out as much area as possible so that the switching node does not interfere with the signals on the source pour. These pours provide low resistance connections for high current tracks.

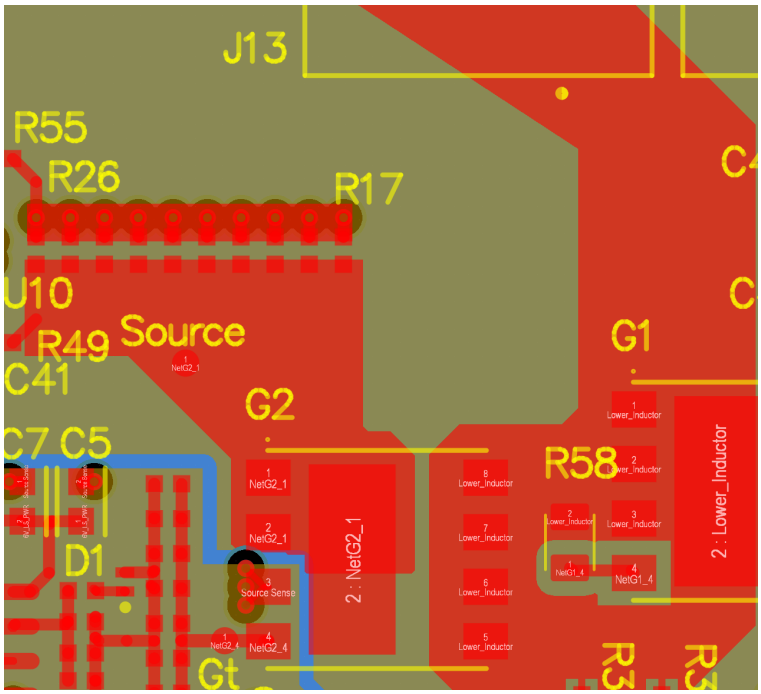

Figure 16. Red polygon pours for the drain and source of the GaN FET DUT.

We also have three different ground pours for our PCB. There is a signal ground pour for the drive signal controlling the gate driver, an isolated ground pour for the power loop of the DUT, and also a gate loop ground pour since the gate driver power is referenced to the source of the FET. This reference ground allows the gate driver to provide a high enough gate voltage to turn the FET on.

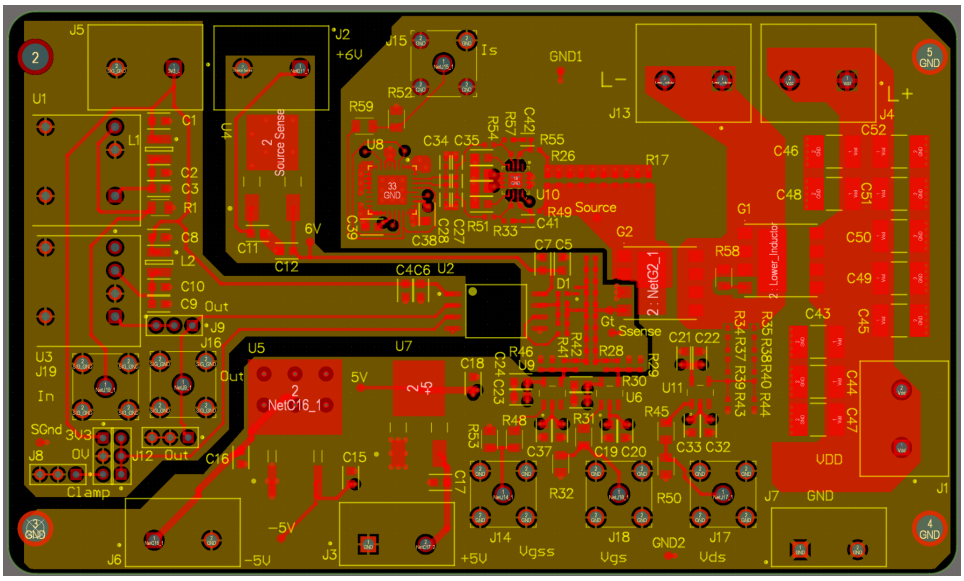

Figure 17. Signal ground (left), gate loop reference ground (middle), power loop ground (right).

Tests and Results

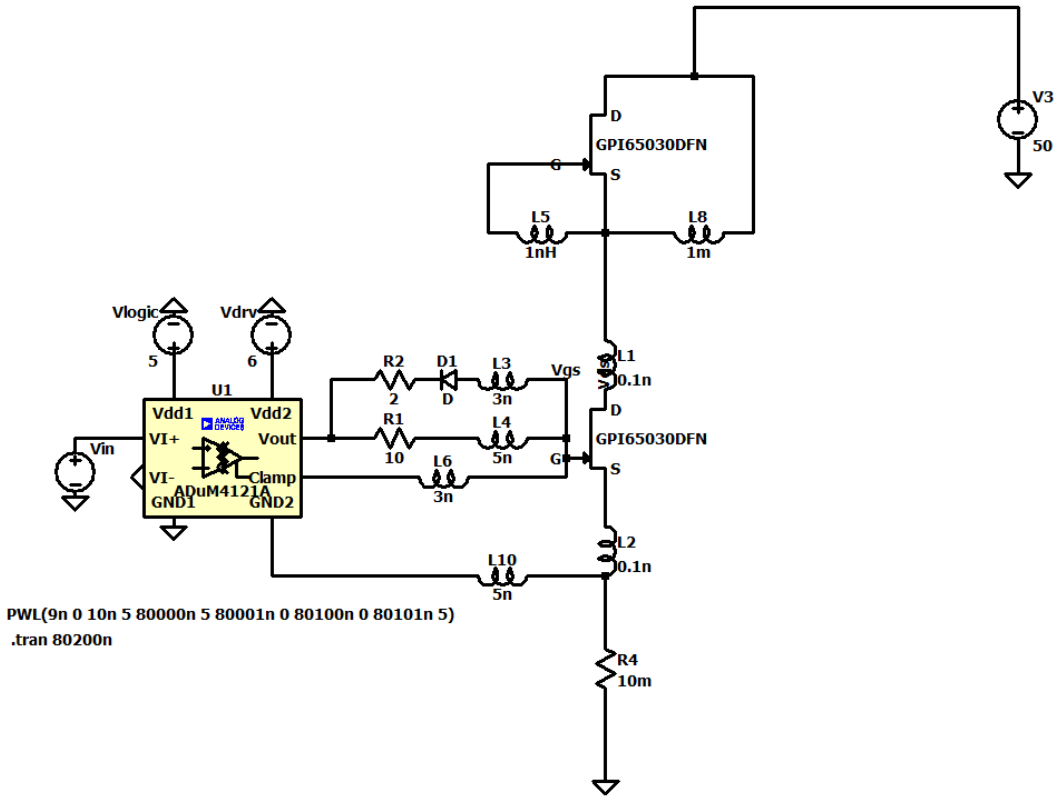

Figure 18. DPT LTspice simulation schematic.

While we were unable to collect real world data in time, extensive testing was done in simulations in LTspice. The DPT was simulated using the proposed driver circuitry and the results are presented below. In the DPT used to generate the plots, an on gate resistance of 10 Ω is used and the off resistance is 10Ω in parallel with a 2Ω resistor with the diode. The 1mH inductor is charged until its current reaches 4A from a V_{DD} of 50V. The instantaneous power loss is found by the positive product of V_{DS} and I_{DS}.

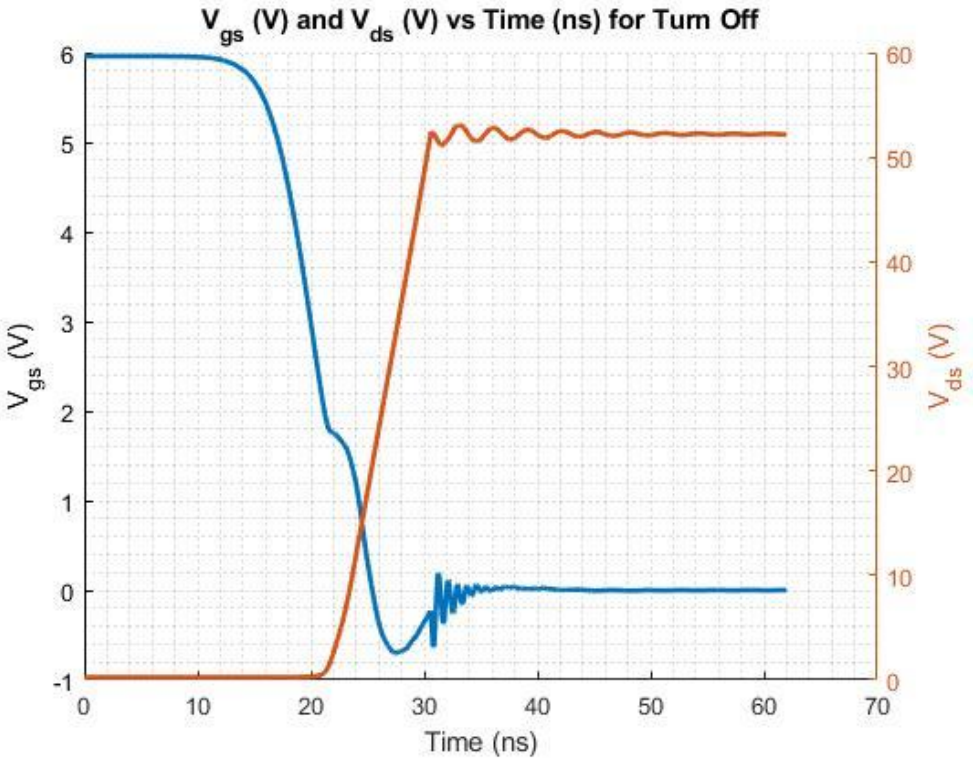

Figure 19. V_{GS} (blue) and V_{DS} (orange) during a turn off cycle.

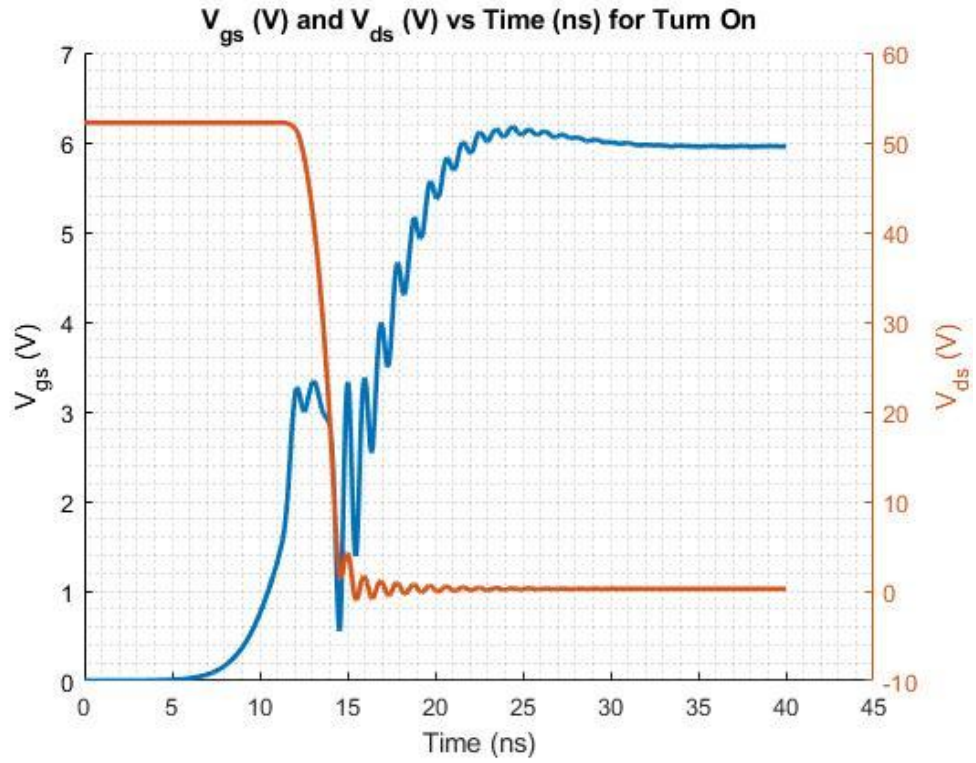

Figure 20. V_{GS} (blue) and V_{DS} (orange) during a turn on cycle.

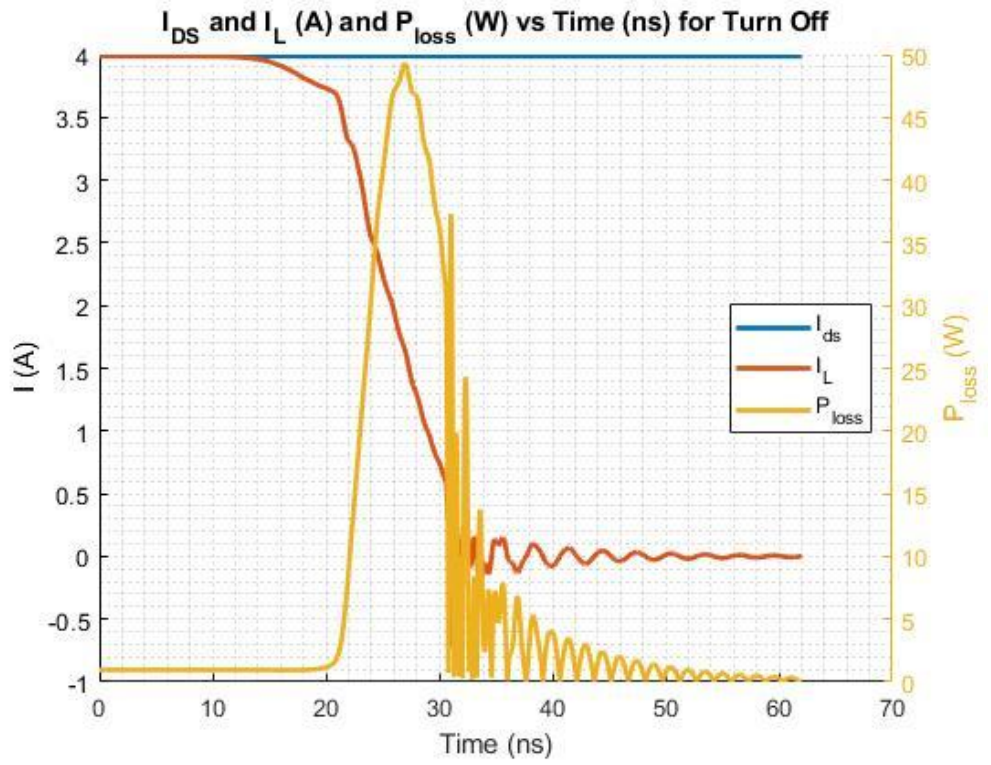

Figure 21. Currents I_{DS} and I_L (inductor current) plotted with switching losses P_{loss} for turn off.

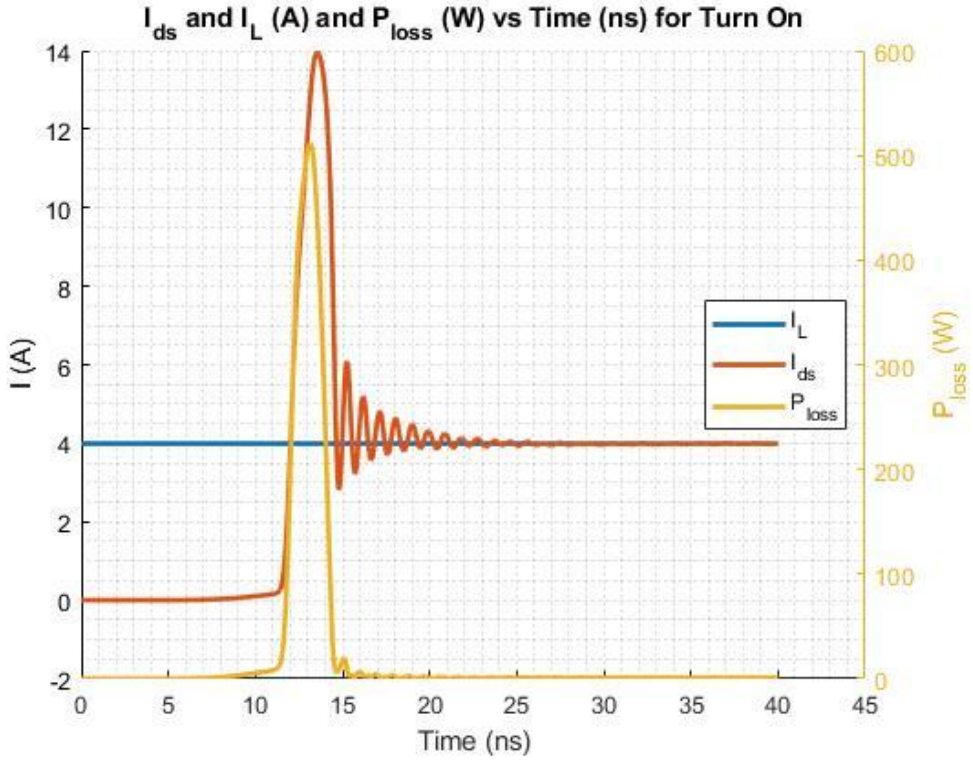

Figure 22. Currents I_{DS} and I_L (inductor current) plotted with switching losses P_{loss} for turn on.

Using a main gate resistance of 10Ω allows for a 11.15ns turn on/off times with minimal V_{GS} overshoot upon turn on accomplishing the goal of fast controlled switching.

Surprisingly the instantaneous switching power loss for turning the FET on is 10x greater in magnitude to the power lost during turn off. As seen in figure 22, this is a result of a large amount of current flowing through the FET. Since the maximum I_{DS} is greater than the inductor current, the top FET is conducting in the forward direction for a short while. This result is surprising since this shoot through is unavoidable in simulation.. Even if the top FET's V_{GS} is held at -6V, the spike is still seen. The spike also does not appear on waveforms from DPTs conducted using other GaN FETs in literature [9]. This leads us to believe that it is likely a result of an inaccurate simulation model of the GaN FET.

The simulated data provides some insight into what waveforms we can expect. It depicts the ringing and overshoot resulting from high speed switching. That is not to say there are no fundamental limitations. The accuracy of the GaN FET model used is unknown and the current parasitic inductances are estimates.

CONCLUSION

Our sponsors are interested in understanding GaN FETs for their research in high speed power electronics, thus their original objective for this project was for us to develop an H-bridge to thoroughly and systematically explore the performance of GaN FETs. This ultimately evolved into our role in this project to focus on the design and use of circuitry to measure and characterize the performance of the FETs.

Unfortunately, due to a combination of shipping and manufacturing delays, our testing circuitry is yet to arrive at the time of writing this report. Thus, our results are based on simulation and research, to later be confirmed using our incoming setup.

Based on our simulation results, we have demonstrated that GaN FETs exceed the parameters to fulfill the requirements for this project. Our simulations show a rise time of 11.15ns can be achieved which strongly suggests that GaN FETs would be adequate for the 1MHz switching speed our sponsors desire.

A significant risk that remains, comes from the lack of physical testing with our systems. We expect to see significant ringing, and other issues that only arise in physical boards, which we have been unable to test yet. Further testing would eliminate this issue.

RECOMMENDATIONS

The immediate next step should be to populate our testing circuitry, and to perform the DPT on the selected GaN FET package. Once the proper experimental data is collected, assuming it has proven the usefulness of GaN FETs, we recommend constructing an H-bridge with these devices. Although we expect that the GaN FETs will operate perfectly in an H-bridge, this hypothesis should still be tested.

In addition, we recommend further robustness testing of the GaN FETs. As they will be switching fast, it is possible that they will deteriorate sooner than expected. As such, an Unclamped Inductive Switching test [10] should be used to test the reliability of the GaN FET in a high stress, turned-off state, or when exposed to switched currents. Similarly, we recommend a Short Circuit test [10] to determine the time in which a GaN FET is destroyed while withstanding a faulty event.

In summary, we are confident based on our theoretical data that GaN FETs are an excellent technology to continue pursuing. Through our testing and research, we have no reason to believe that they will not work for a high switching power electronics application, and recommend confirming this belief further with experimental data.

DELIVERABLES

1. Printed and Populated Testing Circuit Board
    a. Double Pulse Tester
    b. Measurement Circuits
    c. Driver Control Through Optical Fiber
2. Circuit Design Files
    a. GitHub Repo
3. Inductive Load Used for Testing
4. Team Logbook

*Note: As the scope of our project has changed, the list of deliverables no longer includes a functional H-bridge

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APPENDICES

A1: Inductor Design

In order to accurately test and characterize our GaN FETs, we need a load in order to represent what these FETs would see in an end product. Through discussions with our sponsors, it is determined that an inductive load of ~ 1mH would be sufficient.

To create the inductor, materials we had available, including litz wire, ferrite cores and magnetic cores are used. In this process, there are a couple of primary design parameters to keep in mind. Obviously, we need this inductor to be ~ 1mH. As well, it's essential that it is able to operate at a high enough frequency (ideally > 2MHz).

The first factor to keep in mind while designing for high frequency is skin effect. Skin effect increases the effective resistance of a conductor in high frequency applications. As such, it's necessary to use litz wire, or another form of wire designed to minimize this effect. It is likely even better to use a foil wire, once reaching greater than 1MHz.

The second factor is the design of the inductor itself. There are several important things to keep in mind while creating the inductor. The first is to avoid layering the wire. Layering the wire tends to create capacitance between the layers, thus resulting in a higher impedance at high frequency. The second, similarly, is to maintain a gap between the input and output of the inductor. This also results in a lower impedance, and thus a higher possible frequency [18].

A2: Current Measurement Methods

One of the most fundamental measurements in electronics, current measurements, are deceivingly difficult to measure during power electronics applications. The factors at play include measurement bandwidth, added reactances to the current path, power dissipation, measurement isolation, and physical size. Many different current measuring topologies have been developed to specifically address each of these parameters at the cost of others. Consequently, selecting the right one for a specific application can be difficult due to the number of options:

Types	Max Bandwidth	DC	Size	Isolation	Limitations
Shunt Resistor	kHz-MHz	Yes	small	No	Power loss, parasitic inductance
Coaxial Shunt	GHz	Yes	Large	No	Size, parasitic inductance
PCB Coax Shunt [23]	GHz	Yes	small	No	Manufacturability, parasitic inductance
Hall sensor	kHz-MHz	Yes	small	Yes	Bandwidth, noise immunity
Magneto resistor	kHz-MHz	Yes	small	Yes	Bandwidth, noise immunity
Current transformer	MHz	No	Large	Yes	Size, no DC measurement
Rogowski Coil	MHz	No	small	Yes	no DC measurement

Table A2-1. A comparison between current sensing topologies. Table directly taken from [22] with the addition of the PCB coaxial shunt[23].

Each of the topologies shown in the table above can fall into one of two categories: resistive voltage measurements, or magnetic field measurements.

Magnetic field current measurements

The magnetic field measurements leverage the magnetic field generated by the current flowing through a conductor to determine the amount of current flowing through said conductor. This topology is preferable for measurements where isolation is required since there is no shared ground or electrical connections between the measurement circuits and the measured circuits. This isolation also ensures that there are no added parasitics to the DUT which could affect the performance of the device. However, these measurement techniques have low

measurement bandwidths, sometimes barely reaching the low MHz range. Other drawbacks include:

- Requiring additional external active circuitry to convert the measurement into a useful signal which can add complexity to a design.
- Some methods cannot measure DC currents.
- Susceptibility to noise from external magnetic fields
- Often these methods require some tuning to calibrate the measurement

That being said, these measurement methods are excellent options if isolation is required or if the margin for added parasitics is low.

Resistive voltage measurements (Resistive shunts)

The simpler method to measure current is to add a sense resistance in the current path and measure the voltage across the resistor. This method's main draw, aside from the simplicity of the measurement, is the high bandwidth. Using coaxial shunt structures allows for current measurements up into the GHz range. The biggest drawback to these methods is the added inductance and power loss introduced to the DUT from the addition of a resistive element. Although resistive shunts are typically in the range of mΩs, the high current can dissipate significant amounts of power and heat up the resistors in use. It is therefore clear that shunt resistors for high current measurements must have low temperature coefficients of resistance since they will undoubtedly heat up during use.

Perhaps the more damning characteristic of resistive shunts is the added inductance they introduce. By adding a resistor to the current loop being measured, the inductance increases due to the increased size of the new current loop area. In addition, the resistor will have some inductance associated with the physical device structure. And finally, the device which is used to measure the voltage across the shunt may also introduce parasitics to the current loop. Although resistive shunts can achieve the highest bandwidth, there are many issues which can get in the way.

Reducing inductance in resistive current measurements

To reduce the added inductance to the current loop the size of the resistive shunt must be minimized. This will decrease the added size of the current loop which entails a lower inductance. Another way to reduce the inductance is to add several resistive elements in parallel. This will decrease the inductance introduced by the resistors as well.

Ensuring high bandwidth from resistive current measurements

In order to ensure the highest measurement bandwidth off of a resistive element the measurement loop area must be kept small. This means moving the measurement device as close to the shunt as possible. Another technique which is commonly used is to create a spatial region with low magnetic field around the measurement loop area. This ensures that the measurement loop area couples very small amounts of magnetic flux and consequently maintains its high bandwidth. The two methods of achieving a low field region are the flat shunt and coaxial shunt structures.

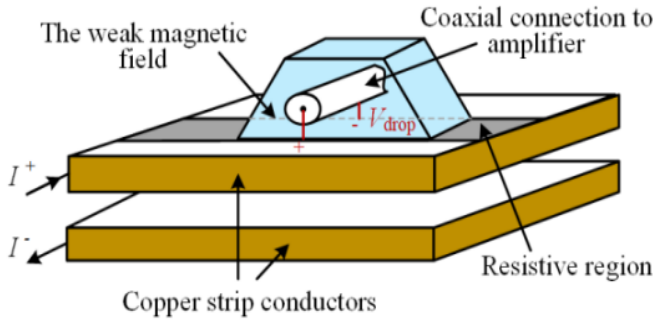

Figure A2-1. A flat shunt structure [22].

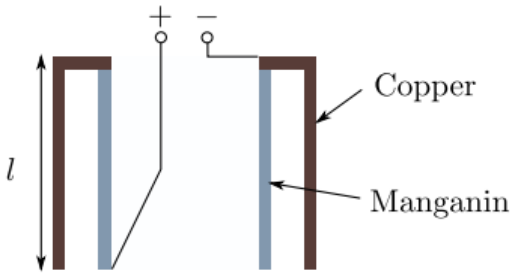

Figure A2-2. A coaxial shunt structure [23].

Both structures take advantage of fundamental physical structures which in ideal cases have regions of zero magnetic field: the stacked infinite plane, and the concentric cylindrical shells. For both of these structures one surface carries the forward current and the other carries the return current. The magnetic fields sum in between these surfaces and cancel everywhere else. For the flat shunt this means current very close to the surface of the device is field free, and for the coaxial structure this is the region inside the shunt. In practice, the coaxial structure achieves superior measurement bandwidth, but the flat shunt is easier to integrate into a circuit and introduces lower added inductance since coaxial shunts cannot integrate easily into PCBs [22,23]. However, a new coaxial shunt resistor which can be built into a PCB has been developed and boasts very low added inductances to the circuit, and high bandwidth [23]. This new technique does have some restrictions in usage due to power dissipation limits.

A3: Capacitor Selection

Due to our high power high speed switching requirements, our DC-Link capacitor selection for our double pulse tester is a non-trivial task. To properly select capacitors for this application we need to be aware of parasitic inductances, voltage ratings, and overall capacitance of each capacitor.

Capacitors are RLC circuits

When a designer adds a capacitor to their circuit, they believe they are adding a pure capacitance. In reality, due to the physical nature of capacitors there is some inherent inductance and resistance associated with it that cannot be avoided. To understand why this parasitic inductance is such a big deal we must examine the impedance of an ideal capacitor and inductor in the frequency domain.

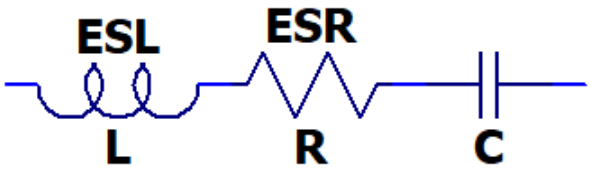

Figure A4-1. The equivalent circuit for a real capacitor.

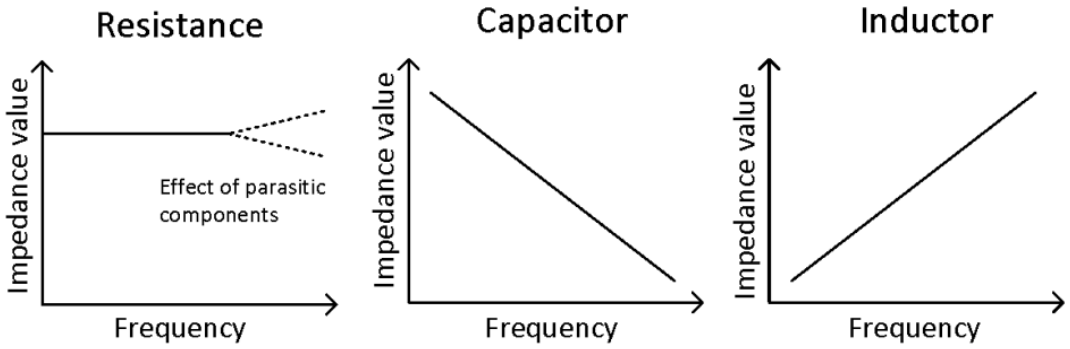

Figure A3-2. The impedance of a capacitor, inductor, and resistor versus frequency image. Source: Impedance measurement handbook 1st ed. Hioki.

Starting from DC, the impedance of a capacitor is infinite, and as the frequency decreases the impedance drops according to x^{-1}. Inversely, the impedance of an inductor is 0 at DC, and as the frequency increases the impedance does as well. And finally, for a pure resistive element with no parasitics the impedance is constant across all frequencies. All these impedances can be seen in figure A4-2. When we select a capacitor to add to a circuit, with the

intention of adding capacitance, we are actually adding a series RLC circuit (see figure A4-1) with an equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance. The impedance of this RLC circuit will depend on the relative values for each of these circuit elements, and which frequency the circuit is operating.

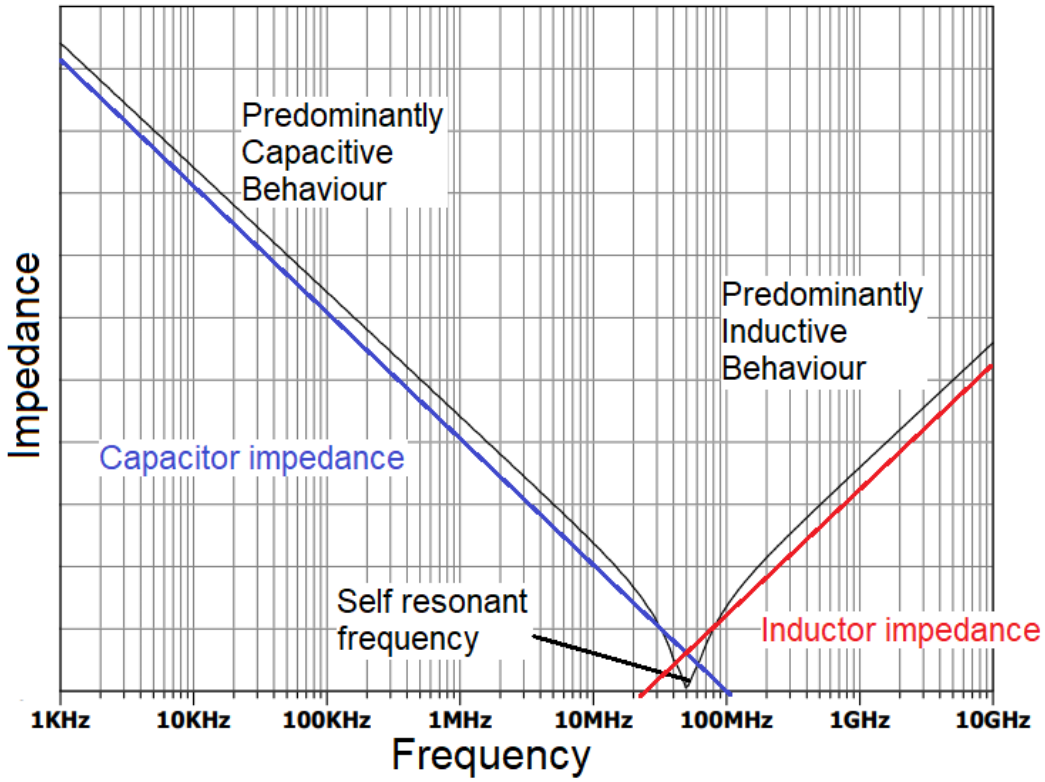

Figure A3-2. A typical impedance profile of an RLC circuit

A typical RLC impedance profile overlaid with a red and blue curve that represent the impedance of a pure inductor and pure capacitor can be seen in figure A4-2. We can see from this graph that for lower frequencies the impedance of the circuit looks predominantly like a capacitor, and that for higher frequencies it looks like an inductor. But right at the frequency in between these regions the impedance reaches a minimum value. This is the resonant frequency of the RLC circuit, or the frequency at which the capacitor impedance is equal to the inductor impedance. At this frequency the inductor and capacitor cancel each other out so the impedance seen at this frequency is just the resistance. Since our capacitor is an RLC circuit, and since we want our capacitor to be adding capacitance to our circuit, we want to select capacitors which have resonant frequencies higher than the highest frequency seen in our circuit. This way, we are sure that we are adding predominantly capacitive elements and not inductive ones.

If we were to decrease the capacitance of the capacitor in a RLC circuit, graphically we would be moving the blue curve downward since higher capacitances have lower impedances. If this happened the resonant frequency would shift to lower frequencies. The same thing would occur if we increased the inductance, since this would move the red curve upwards. So if we want to have a capacitance at high frequency, we need to minimize the inductance but also decrease the capacitance of the capacitor. This is counter intuitive, since we need to make our capacitance smaller to be able to use the capacitance at high frequency. So in practice, we try to add the largest capacitor with the smallest inductance which allows for our desired capacitive frequency range.

Inductance of capacitors

Figure A3-3. Several different capacitor packages of different sizes

Inductance, just like capacitance, is a product of the physical dimensions of a device. Analysis of an arbitrary shape to determine its intrinsic capacitance and inductance is very difficult and requires complicated calculations. But since commercially available capacitors come in standardized sizes we can discuss the relative inductances between packages. A quick rule of thumb to select a low inductance capacitor is to choose the widest, shortest, thinnest package possible. The smallest packages are the surface mount capacitors which can barely be seen in the bottom center of figure A3-3.

For our specific design we aimed for a maximum switching frequency of 1MHz which translates into a minimum capacitive self resonant frequency of at least 35MHz. In addition, our calculations determined that we would need at least 1uF of capacitance for our double pulse tester circuit. 1uFs is a lot of capacitance, and 35MHz is a high self resonant frequency. This immediately limited us to select from surface mount components due to their lower inductances from the smaller sized packages. However, since we also wanted to have high power, and high voltage, operation of our circuit we also needed to pay attention to voltage derating.

Voltage derating of capacitors

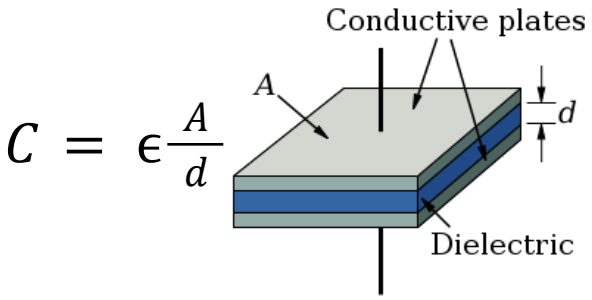

Figure A3-4. A parallel plate capacitor. Source: Wikipedia commons.

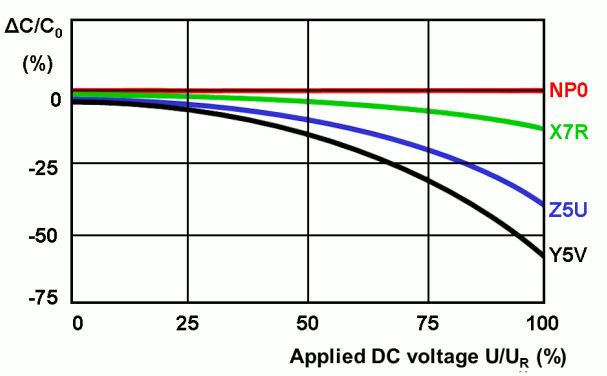

Figure A3-5.Capacitive derating for different dielectrics. Source: Wikipedia commons.

Capacitors are, in the most basic terms, metal plates with dielectric between them. The dielectric between the plates is what gives the capacitor its capacitance. A material property which is directly proportional to the capacitance of a capacitor is the relative permittivity ε. For an ideal dielectric, ε is a fixed constant and never changes. In the real world it is not so. The relative permittivity of a dielectric is a function of the electric field applied through it and by extension the voltage applied across it. This means that the capacitance will decrease as we increase the voltage across the capacitor, eventually dropping to a fraction of its initial capacitance. To avoid this drop-off when using high voltages, high quality dielectrics with low voltage dependance ε's must be used.

By combining all of these requirements, we can build a shopping list of qualities we want our capacitors to have:

1. Low inductance. This means higher resonant frequency so the capacitors are capacitive for higher frequencies
2. High quality dielectrics. This means low voltage derating for high power use.
3. High capacitance per capacitor. Want to get a significant amount of capacitance for our circuit and we have a finite amount of space to place these capacitors

Capacitors with all these qualities can be bought at a significant cost. Even then, they are limited to 100s of nF of capacitance per device and can cost several dollars per capacitor. Most capacitor manufacturers have their own line of capacitors which are specifically designed for high speed high power applications like our double pulse tester. The final requirement we used to choose our capacitors was available stock.

A4: GaN FET Physics

Gallium nitride (GaN) as a standalone semiconductor does not have amazing material properties across the board. In fact, there are actually several fundamental material characteristics which silicon has that are superior to those of GaN. However, due to the device topologies that can be built with gallium nitride in coordination with other materials, GaN becomes a revolutionary material for power electronics and GaN FETs are a revolutionary device.

As we have previously motivated, an ideal transistor for power electronics should have the following qualities:

- Low conduction losses
- Low switching losses
- High voltage ratings
- Strong thermal properties
- Small size

To understand how GaN allows the creation of switching devices with all of these qualities, we must explore the physics behind the material and device structure employed in these device

Physical properties of GaN vs Silicon

	Silicon	Gallium nitride
Bandgap (eV)	1.12	3.4
Critical Electric Field (MV/cm)	0.3	3.3
Relative permittivity	11.8	8.9-9
Carrier Mobility (cm^2/Vs)	1400*	990/2000**
Thermal conductivity (W/cm^2K)	1.5	1.3

**in un-doped silicon, **Carrier Mobility increased in 2DEG region*

Table A4-1. Material properties of Silicon and GaN [3,4,5,7,13].

To build superior devices we require superior materials, and GaN has many material properties which make the material preferable over silicon for power electronics applications. These properties allow for the construction of high power and high efficiency transistors. The following sections will go through how the material properties of GaN lend themselves to better devices.

V_{DS} breakdown voltage

GaN belongs to a group of materials called a wide bandgap semiconductor. In electrical terms, this means that to get GaN to act as a conductor a larger voltage must be applied to the material when compared with a normal semiconductor like silicon. This phenomenon is captured by the critical electric field.

Critical electric field

The critical electric field, in units of MV/cm, is the maximum electric field that can be applied to an insulating material before the material begins to conduct. When the critical electric field is applied to a material a current is forced through the material which can cause catastrophic device failure. As we can see from the units of an electric field, volts per length, if we want a certain material to withstand a certain applied voltage we can use the critical electric field to determine how large this material would need to be to avoid failure due to the material breakdown.

For power electronics devices we want as high of an critical electric field as we can achieve since this allows for higher V_{DS} breakdown voltages, which is the voltage at which the transistor fails by short-circuiting the drain to the source. The V_{DS} voltage rating is one of the primary constraints, along with power dissipation, which affects the device size. Using a material which has a larger critical breakdown field means smaller devices. The critical electric field for GaN is 10 times larger than silicon. This translates to a GaN FET chip being 10 times smaller than a silicon device with the same voltage rating [11].

Parasitic capacitances

We have already seen that due to the higher critical electric field of GaN we have a significant size reduction of the device. We know reducing the size will reduce the parasitic capacitances of a device. However, choosing proper materials can also have an effect on the magnitude of these parasitics.

Relative permittivity

The relative permittivity of a material affects the strength of an electric field within the material relative to a vacuum. The effect of a higher relative permittivity material being used in a device is higher parasitic capacitances. To see this we can look at the equation for a parallel plate capacitor filled with a dielectric with relative permittivity ε:

$$C = \epsilon \frac{A}{d}$$

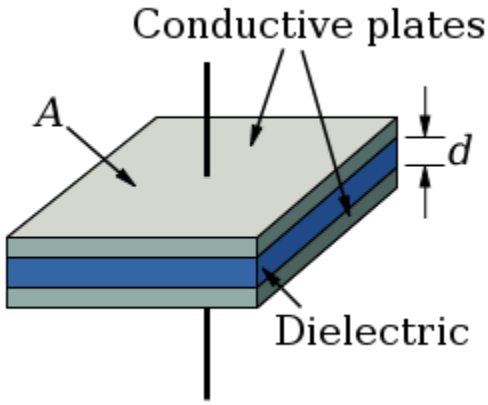

Figure A4-1. A parallel plate capacitor. Source: Wikipedia commons.

As we can see from the equation, the capacitance is linearly proportional to the dielectric constant of the material and the area of the capacitor. So a device made of a material with a lower dielectric constant and a smaller size will have much lower parasitic capacitances. We already have a significant capacitance reduction going from GaN to silicon due to the size reduction from the larger critical electric field. But, we have a further reduction due to GaN's lower dielectric constant. This contributes to GaN devices' super fast switching characteristics which leads to its lower switching losses. In commercially available GaN FETs the parasitic input capacitances can be up to 30 times lower than that of silicon MOSFETs and partially due to this reduction in capacitance the operating frequency of GaN FETs are roughly 30 times higher than silicon MOSFETs [11].

Current carrying capacity

Fundamentally, all transistors are devices which move charge carriers from one place to another. The faster the charges are moving across a device, the higher the current is flowing through the device. To make these charge carriers move some force must be applied to them. A material property which captures how hard of a push is needed to move a charge carrier is the carrier mobility.

Carrier mobility

Carrier mobility, units of cm^2/Vs or velocity over electric field, is a measure of how strong an electric field is required to move an electron at a given speed. Carrier mobility is one of the material properties, along with carrier concentration, which contribute to electrical conductivity of a material: a high carrier mobility means a small voltage needs to be applied to induce a charge

carrier to move at high speed which leads to higher currents through the material. It then follows that a good transistor would have high carrier mobility since it would allow the device to have high conduction. In addition to the current carrying capacity, high carrier mobility also leads to higher switching speeds [11].

The carrier mobility of pure GaN (990cm²/Vs [7]) is actually quite low compared to silicon (1400cm²/Vs [7,11]). However, by taking advantage of other material properties of GaN and some clever device architecture we can increase the carrier mobility up to 2000cm²/Vs [7,11]. This means that GaN will have an edge over silicon in terms of carrier mobility and, as we will see in a moment, GaN also has a significantly higher carrier concentration [1,12] which results in conduction several orders of magnitude higher than silicon. This higher conduction value means a higher current carrying capacity for GaN devices and a lower power dissipated due to conduction losses.

Thermal considerations

Devices which are used in high power applications need to be able to stay cool. If a device gets too hot they can break or change their properties in a way which degrades system performance. Consequently, lots of attention is directed to the thermal characteristics of power transistors.

Thermal conductivity

To avoid temperature rise in a device, a material with a high thermal conductivity is preferable. This allows for the heat generated in the device to be efficiently spread out away from the device which results in a lower peak temperature.

The thermal conductivity of GaN is very slightly lower than silicon (1.3 vs 1.5 W/cm²K) [7,11]. However, due to the reduced losses from the other material properties of GaN (lower conduction and switching losses), GaN devices heat up less during use. A reduction in heat generated also means a reduction in device size. This is because devices which generate more heat need to be larger to accommodate the need for higher power dissipation.

We can see that due to all these material properties GaN is better suited for building FETs than silicon. Now to make the most out of this material we must design the devices to get the most out of the material.

The HEMT structure

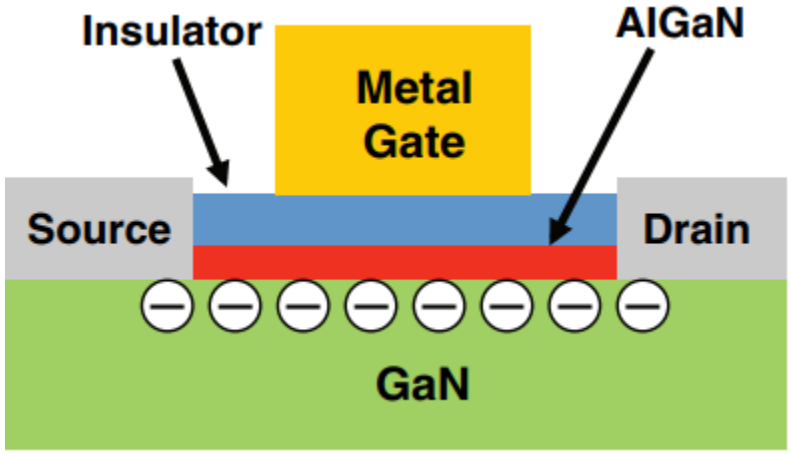

Figure A4-2. A diagram highlighting the physical structure of a GaN HEMT [13].

We have seen that GaN is superior to silicon for use in power electronics. However, for this material to be useful we require an actual device which properly utilizes the advantages of the material. One structure which can be used to make a GaN FET is that of the basic High Electron Mobility Transistor (HEMT) which can be seen in figure A4-2. This architecture takes advantage of a phenomena called the 2-Dimensional Electron Gas (2DEG) which forms at the interface between two semiconductors with dissimilar bandgap energies. Using a HEMT is functionally the same as a regular FET - by controlling the voltage at the gate the device can be switched on or off. The structure shown in figure A4-2 is a normally on HEMT but normally off devices also exist. A HEMT switches off by breaking up the 2DEG region by removing electrons directly below the gate from the channel by applying an electric field.

2DEG

The 2DEG region is a thin volume at the junction between two semiconductors with dissimilar bandgap energies which contains a high density of free electrons which also have very high mobility within the region [11]. Using GaN with AlGaN forms this 2DEG region at the point where these materials are in contact. The HEMT structure and the 2DEG region not only takes advantage of GaN's excellent material properties, but also improves on them. As we have mentioned before, the carrier mobility of pure GaN is actually lower than silicon. When we form a 2DEG region we get roughly double the carrier mobility of our pure GaN while also achieving

a high carrier concentration (~10^{17}/m² electrons in the GaN 2DEG [1,12]). All of this combines to make the conduction of GaN HEMTs several orders of magnitude higher than silicon.

On Resistance (R_{ON})

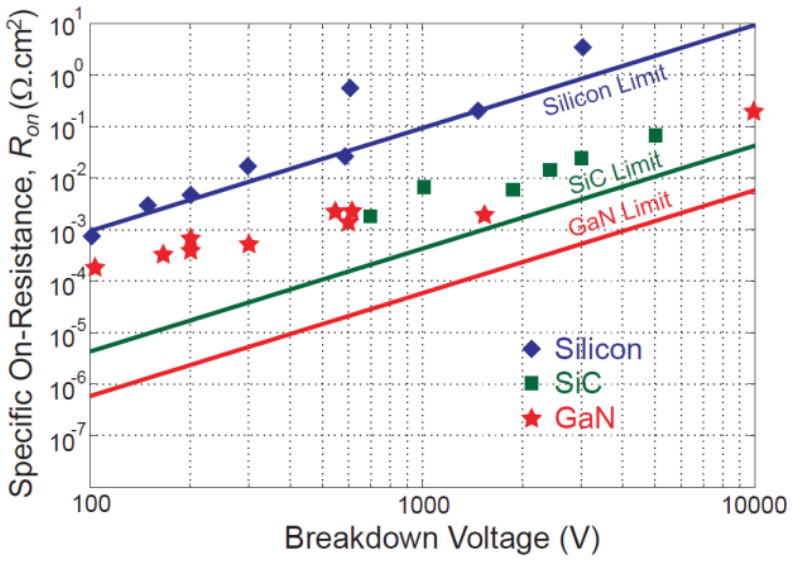

Figure A4-3. The relation between R_{ON} and breakdown voltage of a device for a given material [15].

Since the 2DEG gives the GaN HEMTs a very high conduction value, this means the devices have very low resistance when conducting. The transistor parameter which describes the resistance while conducting is the R_{ON}, or the resistance from the drain to source of the device while on. This resistance is a function of the device structure and materials, but also a function of length of the conducting channel. The main parameter which affects the length of the conducting channel is the breakdown voltage (which is a function of the critical electric field, see previous section).

Using the inherent conduction value for different materials per unit length we can determine the lowest possible resistance for a power transistor as a function of the breakdown voltage. This is represented graphically in figure A4-3. The graph shows silicon, silicon carbide (another less popular transistor material), and GaN. We can see from the figure that in theory the on resistance of a GaN FET is three orders of magnitude lower than silicon. The significant reduction in on resistance is due to leveraging the 2DEG region for its high conduction properties.

Reverse conduction

Another advantage of using the HEMT structure is the ability to conduct in reverse. If we examine the GaN HEMT structure we can see that it is symmetric about the gate. This symmetry manifests itself in GaN HEMTs ability to conduct in both directions (drain to source or source to drain) as long as the 2DEG is unbroken. This reverse conduction property is very useful for any circuit designer since it adds flexibility to how the device can be used. Silicon power MOSFETs do have a similar property where they can conduct backwards. However, this property is not pure reverse conduction since silicon MOSFETs have a voltage drop associated with them when they conduct backwards due to a parasitic body diode which is built into the device. GaN HEMT reverse conduction operates exactly the same as forward conduction and therefore has no voltage drop while it conducts in reverse.

Physics Summary

Gallium nitride has material properties which allow for the construction of GaN High electron mobility transistors (HEMTs) which are superior to silicon MOSFETs. The GaN HEMTs are smaller due to the higher critical electric field and better thermal characteristics of GaN HEMTs, can switch faster due to the smaller device size and lower relative permittivity of GaN, have much higher conduction because of the 2-Dimensional Electron Gas region in the HEMT structure, and have more versatile functionality compared to MOSFETs due to their reverse conduction properties from the HEMT structure.

A5: Optocoupler

Our sponsors expressed early on the desire to control the FET switching at large distances from the actual FET using optical fiber. Thus, an optical fiber transmitter (Tx) and receiver (Rx) were embedded on the DPT PCB to test integration between the driver and the optical receiver. The AFBR-1624Z and AFBR-2624Z were chosen as Tx and Rx respectively. The particular IC's were chosen as they were simple to integrate with the driver and provided the necessary speed for 1MHz driving.

The driver does not have to be controlled through the Tx and Rx optical fiber circuit. The drive signal can also be injected straight to the driver input by SMA J16 or header J10. If the optical fiber is bypassed, the jumper on header pins J9 should be removed to disconnect the output of the optical Rx from the driver input.

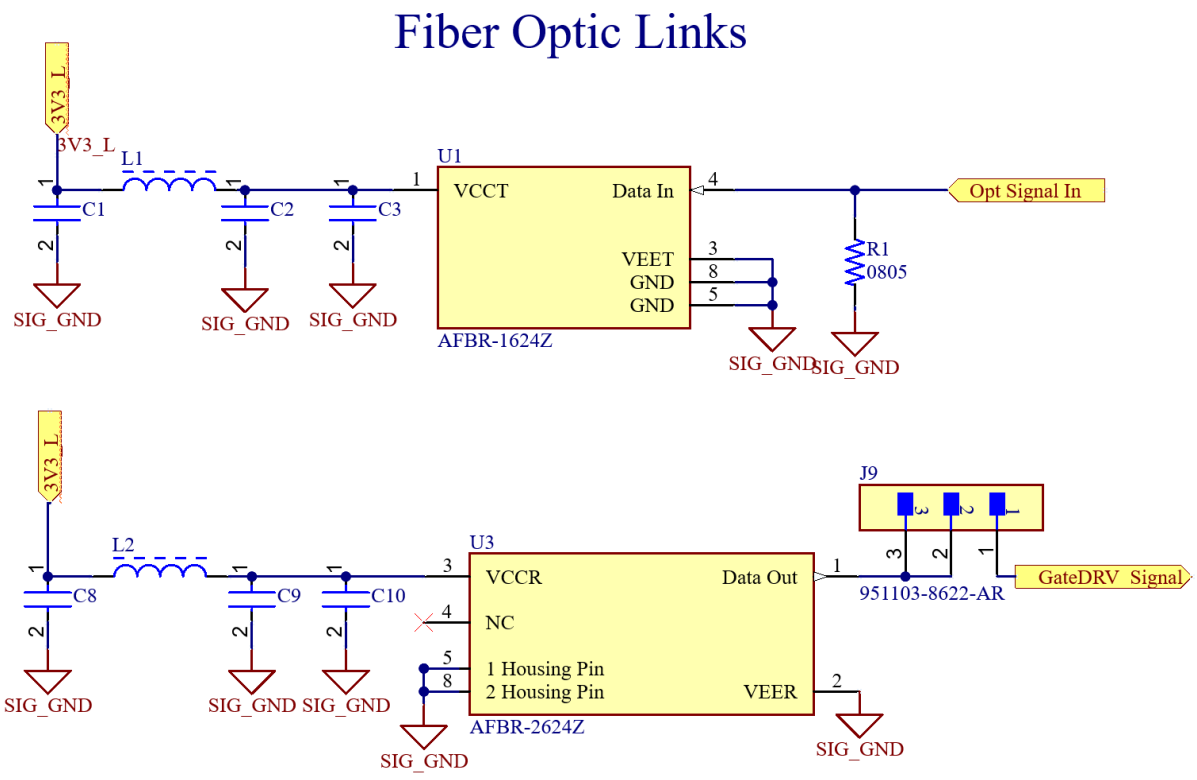

Figure A5-1. Fiber optic link schematic.

A6: Schematic

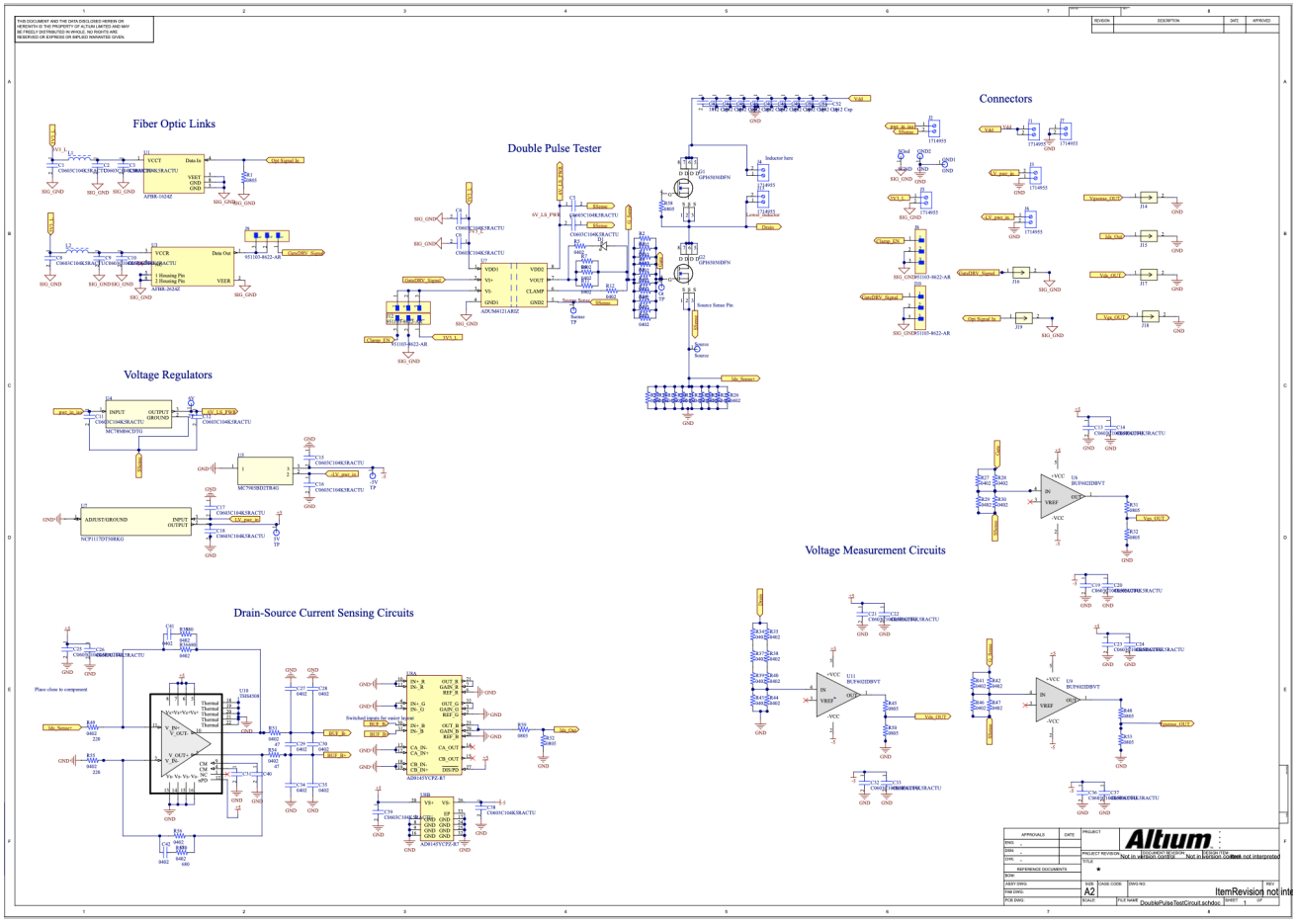

Figure A6-1. Full schematic for reference.

A7: Board Overview

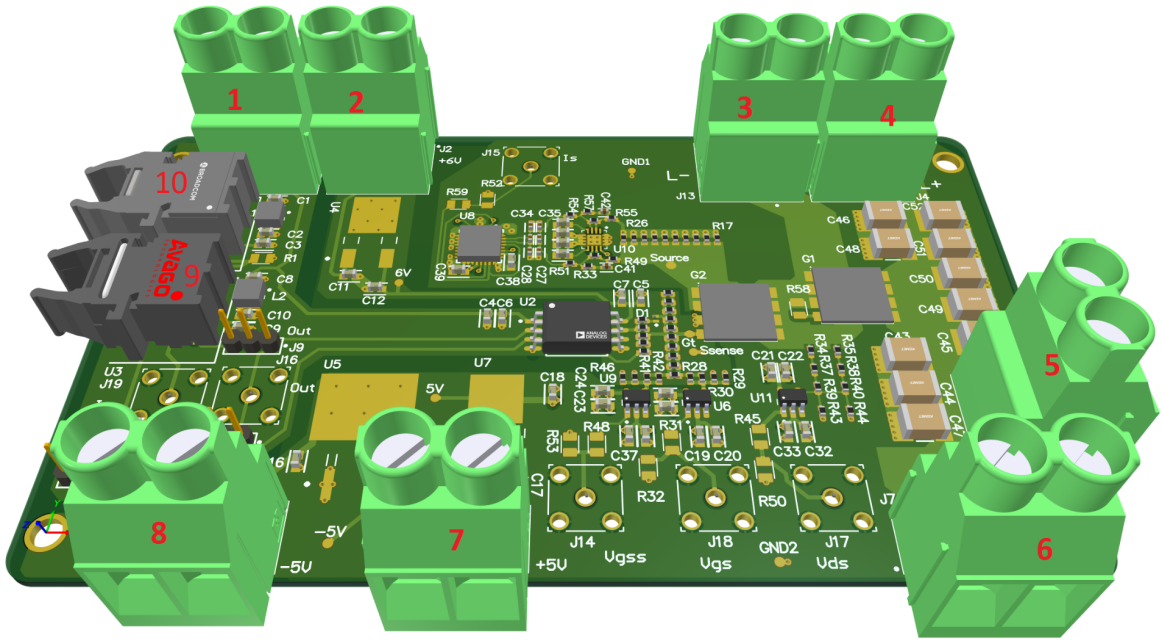

Figure A7-1. 3D view of the final PCB.

Components highlighted in figure A7-1 are explained below.

1. 3V3 power
2. 6V power
3. Lower offboard inductor (pins are shorted together)
4. Upper offboard inductor (pins are shorted together)
5. V_{DD} (pins are shorted together)
6. Power ground (pins are shorted together)
7. 5V power
8. -5V power
9. Fiber Optic Rx
10. Fiber Optic Tx

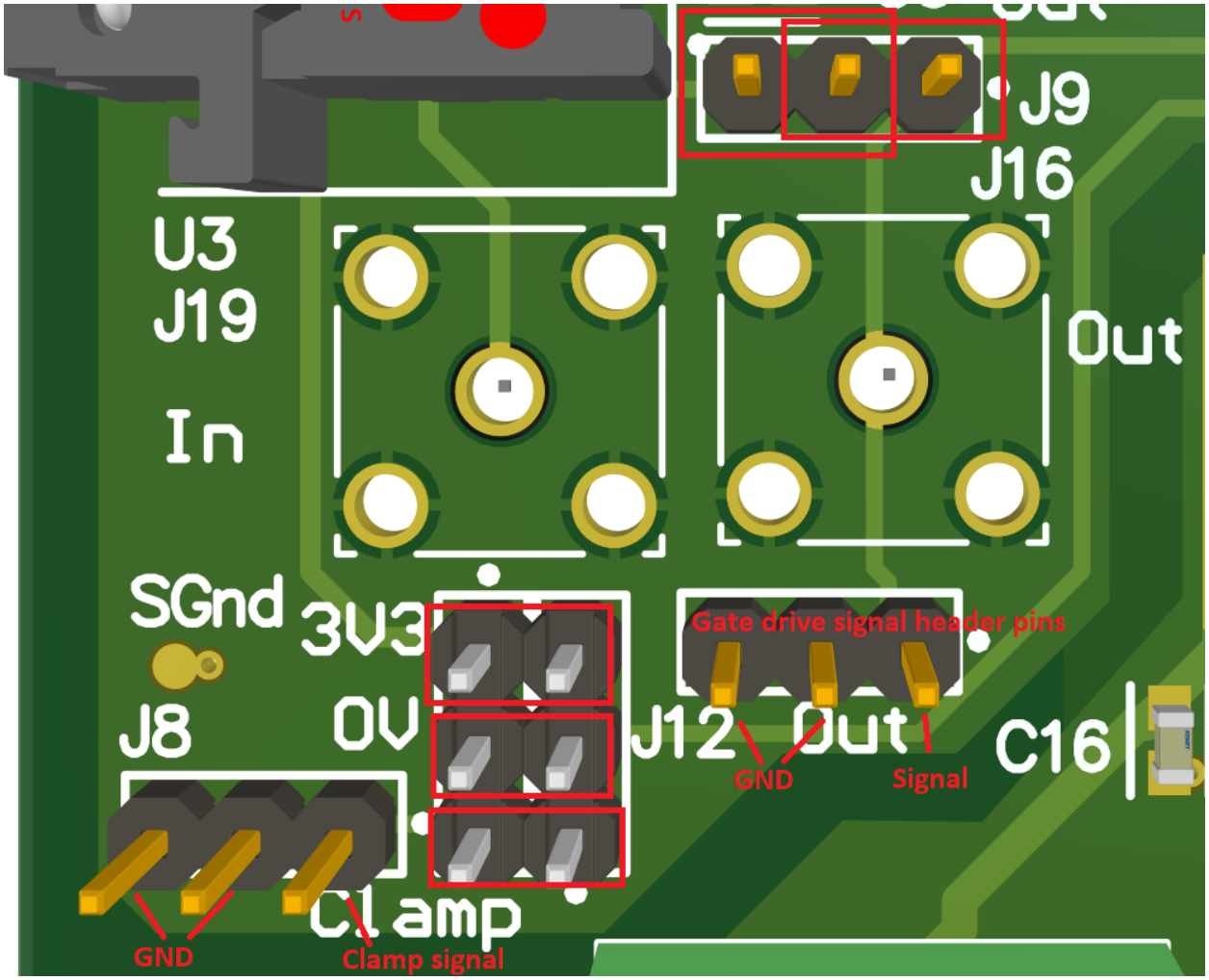

Figure A7-2. Various head pin configurations.

To provide a gate drive control signal, we have three ways to do so. There is a SMA connector (component J16), header pins (component J12), and a fiber optic link (via another SMA connector, component J19). In order to use the fiber optic link, the two rightmost pins on component J9 must be connected. There is also an inverting gate drive logic input which is controlled with a set of header pins as shown on the bottom left of figure A7-2. We have conveniently placed a 3V3 and 0V logic level line, but a different control signal can be used by connecting to component J8 and jumping the bottom row designated with “Clamp”.

A8: Parasitics

Circuit schematics and circuit theory often depicts ideal components. These components have simplified properties and behave exactly as intended. In reality, all real world circuit components have some amount of capacitance, inductance, and resistance associated with them. These unwanted aspects of components are known as parasitics.

For high performance designs where high frequency, high power, or high precision is required, mitigating these parasitics becomes paramount to the success of a design. Various parasitic elements are encountered in this report and their effects are explained.